WHAT IS CLAIMED IS:

1. A circuit, comprising:

a differential amplifier;

a capacitor coupled to an output of the differential amplifier;

an inverter coupled to the capacitor; and

a biasing circuit coupled between the capacitor and the inverter.

2. The circuit as recited in claim 1, wherein the inverter comprises a p-channel transistor coupled in series with an n-channel transistor.

3. The circuit as recited in claim 1, wherein the capacitor comprises a pair of conductive terminals separated by a dielectric, and wherein a first terminal of the pair of terminals is coupled to the output of the differential amplifier and a second terminal of the pair of terminals is coupled to the inverter.

4. The circuit as recited in claim 1, wherein the inverter comprises a gate terminal coupled to the capacitor.

5. The circuit as recited in claim 1, wherein the biasing circuit comprises a transmission gate consisting of a p-channel transistor coupled in parallel with an n-channel transistor.

6. The circuit as recited in claim 5, wherein a gate terminal of the p-channel transistor is coupled to a ground supply voltage and a gate terminal of the n-channel transistor is coupled to a power supply voltage during operation of the circuit.

7. The circuit as recited in claim 5, wherein a gate terminal of the p-channel transistor is coupled to a power supply voltage and a gate terminal of the n-channel transistor is coupled to a ground supply voltage during power down of the circuit.

8. The circuit as recited in claim 1, wherein the biasing circuit comprises a second inverter.

9. The circuit as recited in claim 8, wherein the second inverter comprises both an input and an output coupled to the capacitor.

10. The circuit as recited in claim 8, wherein the inverter comprises a first p-channel transistor and an first n-channel transistor having substantially the same gate length but having a first p-channel gate width at a first ratio relative to first n-channel gate width, and wherein the second inverter comprises second p-channel transistor and a second n-channel transistor having substantially the same gate length but having a second p-channel gate width at a second ratio relative to a second n-channel gate width, and wherein the first ratio is approximately equal to the second ratio.

11. A receiver, comprising:

a pair of inverters;

a biasing circuit coupled to an input of each of the pair of inverters to bias a voltage on the pair of inverters to a trip point of the inverters;

a differential amplifier adapted to receive a differential input signal forwarded to the receiver from a transmission medium; and

a pair of capacitors coupled between the pair of inverters and respective pair of outputs of the differential amplifier to place upon each of the pair of inverters changes in voltage centered around the trip point, wherein the changes in voltage correspond to changes in amplitude of the differential input signal.

12. The receiver as recited in claim 11, wherein each of the pair of inverters is a complementary metal oxide semiconductor (CMOS) inverter.

13. The receiver as recited in claim 11, wherein the biasing circuit comprises a transmission gate coupled between the input and output of each of the pair of inverters to maintain a direct current (DC) voltage bias on the input of each of the pair of inverters approximately at the trip point of the inverters.

14. The receiver as recited in claim 11, wherein the transmission gate comprises a a p-channel transistor coupled in parallel with an n-channel transistor, wherein, during operation, a gate terminal of the p-channel transistor is coupled to a ground supply voltage and a gate terminal of the n-channel is coupled to a power supply voltage, and wherein during non-operation, the gate terminal of the p-channel transistor is coupled to the power supply voltage and a gate terminal of the n-channel is coupled to the ground supply voltage.

15. The receiver as recited in claim 11, wherein the biasing circuit comprises a second inverter having an input coupled to an output of the inverter and also having an output coupled to an input of the inverter.

16. The receiver as recited in claim 15, wherein the ratio of gate widths p-channel and n-channel transistors of the inverter and the second inverter are substantially equal.

17. The receiver as recited in claim 15, wherein the second inverter comprises a four-input inverter, with two inputs coupled to receive a power supply voltage and a ground supply voltage.

18. A method for translating voltages of a differential signal to complementary metal oxide semiconductor (CMOS) voltages, comprising:

biasing an input of a CMOS inverter to a trip point at which the a voltage on the input of CMOS inverter substantially equals a voltage on the output of the CMOS inverter;

coupling onto the CMOS inverter an alternating current (AC) component of the differential signal absent a direct current (DC) component of the differential signal; and

switching the inverter output to CMOS voltage levels whenever the AC component causes the voltage on the biased input of the CMOS inverter to exceed or become less than the trip point of the inverter.

19. The method as recited in claim 18, wherein the biasing comprises maintaining a previous AC component of the differential signal onto the biased input of the CMOS inverter during times when the differential signal is removed.

20. The method as recited in claim 18, wherein the biasing is removed and driven to a ground supply voltage during times when the differential signal is absent.